Claims:

1. An apparatus for transporting a synchronous or plesiochronous signal over a packet network, comprising:

a) a packet processor having an adjustable clock generator;

b) a received packet counter generating a received packet count;

c) a transmitted packet counter generating a transmitted packet count; and

d) a clock adjustment means coupled to said adjustable clock generator, said received packet counter, and said transmitted packet counter, such that said adjustable clock generator is adjusted to a higher rate when said transmitted packet count is smaller than said received packet count.

2. An apparatus according to claim 1, wherein:

said clock adjustment means includes

subtraction means coupled to said received packet counter and said transmitted packet counter for subtracting said transmitted packet count from said received packet count, and

register means for storing the difference calculated by said subtraction means,

said adjustable clock generator being adjusted an amount proportional to said difference.

3. An apparatus according to claim 2, wherein:

said clock adjustment means includes multiplication means coupled to said subtraction means and said register means such that the difference calculated by said subtraction means is multiplied by said multiplication means before being stored in said register means.

4. An apparatus according to claim 3, wherein:

said multiplication means is adjustable.

5. An apparatus according to claim 4. wherein:

said multiplication means multiplies the difference calculated by said subtraction means by 2^n where n is adjustable.

6. An apparatus according to claim 5, wherein:

n is adjustable to an integer value from 3 to 0.

7. An apparatus according to claim 5, wherein:

said clock adjustment means includes derivative means coupled to said register means for detecting change in the difference calculated by said subtraction means, said derivative means having an output indicating the change in the difference calculated by said subtraction means over time.

8. An apparatus according to claim 7, wherein:

said clock adjustment means includes

comparator means coupled to said derivative means for detecting a change in sign of the output of said derivative means, and

decrementer means coupled to said comparator means and said multiplication means such that n is decremented based on the change in sign of the output of said derivative means.

9. An apparatus according to claim 8, wherein:

n is decremented by 1 after a predetermined number of changes in sign of the output of said derivative means.

10. An apparatus according to claim 8, wherein:

said clock adjustment means includes doubler means coupled to said received packet counter and said transmitted packet counter, such that said received packet count and said transmitted packet count are doubled each time n is decremented.

11. A method for transporting a synchronous or plesiochronous signal over a packet network, comprising:

a) processing packets with an adjustable clock generator;

b) keeping a count of the number of received packets;

c) keeping a count of the number of transmitted packets; and

d) adjusting the adjustable clock generator to a higher rate when the number of transmitted packets is smaller than the number of received packets.

12. A method according to claim 11, wherein:

said step of adjusting includes

subtracting the transmitted packet count from the received packet count,

storing the difference calculated by the subtraction, and

adjusting the adjustable clock by an amount proportional to the difference.

13. A method according to claim 12, wherein:

said step of adjusting includes

multiplying the difference calculated by the subtraction before storing the difference.

14. A method according to claim 13, wherein:

said step of multiplying includes adjusting the multiplication factor.

15. A method according to claim 1. wherein:

said step of multiplying includes multiplying by 2^n where n is adjustable.

16. A method according to claim 15, wherein:

n is adjusted to an integer value from 3 to 0.

17. A method according to claim 15, wherein:

said step of adjusting includes detecting change in the difference calculated by the subtraction.

18. A method according to claim 17, wherein:

said step of adjustment includes

detecting a change in sign of the change in the difference calculated by the subtraction, and

decrementing n based on the change in sign.

19. A method according to claim 18, wherein:

n is decremented by 1 after a predetermined number of changes in sign.

20. A method according to claim 18, wherein:

said step of adjusting includes doubling the received packet count and the transmitted packet count each time n is decremented.

21. An apparatus for providing a clock adjustment value in a user-network-interface to a packet network, comprising:

a) a received packet counter generating a received packet count;

b) a transmitted packet counter generating a transmitted packet count; and

d) a clock adjustment value calculator coupled to said received packet counter and said transmitted packet counter for calculating a clock adjustment value based on a comparison of the received packet count and the transmitted packet count.

22. An apparatus according to claim 21, wherein:

said clock adjustment value calculator includes

subtraction means coupled to said received packet counter and said transmitted packet counter for subtracting said transmitted packet count from said received packet count, and

register means for storing the difference calculated by said subtraction means,

said clock adjustment value being an amount proportional to said difference.

23. An apparatus according to claim 22, wherein:

said clock adjustment value calculator includes multiplication means coupled to said subtraction means and said register means such that the difference calculated by said subtraction means is multiplied by said multiplication means before being stored in said register means.

24. An apparatus according to claim 23, wherein:

said multiplication means is adjustable.

25. An apparatus according to claim 24. wherein:

said multiplication means multiplies the difference calculated by said subtraction means by 2^n where n is adjustable.

26. An apparatus according to claim 25, wherein:

n is adjustable to an integer value from 3 to 0.

27. An apparatus according to claim 25, wherein:

said clock adjustment value calculator includes derivative means coupled to said register means for detecting change in the difference calculated by said subtraction means, said derivative means having an output indicating the change in the difference calculated by said subtraction means over time.

28. An apparatus according to claim 27, wherein:

said clock adjustment value calculator includes

comparator means coupled to said derivative means for detecting a change in sign of the output of said derivative means, and

decrementer means coupled to said comparator means and said multiplication means such that n is decremented based on the change in sign of the output of said derivative means.

29. An apparatus according to claim 28, wherein:

n is decremented by 1 after a predetermined number of changes in sign of the output of said derivative means.

30. An apparatus according to claim 28, wherein:

said clock adjustment value calculator includes doubler means coupled to said received packet counter and said transmitted packet counter, such that said received packet count and said transmitted packet count are doubled each time n is decremented.

31. An apparatus for adjusting the granularity of clock adjustments in an interface to a packet network, comprising:

a) a clock adjustment calculator for calculating a raw clock adjustment value based on the flow of packets into and out of the interface;

b) a clock adjustment magnifier coupled to said clock adjustment calculator for magnifying said raw clock adjustment value by an adjustable factor to provide an actual clock adjustment value;

c) first comparison means for comparing a current clock adjustment value with a previous clock adjustment value to provide a clock difference value;

d) magnifier adjustment means coupled to said clock adjustment magnifier and to said first comparison means for adjusting said adjustable factor based on comparisons of clock adjustment values.

32. An apparatus according to claim 31, wherein:

said magnifier adjustment means is a first derivative means for determining the rate of change in clock adjustment values over time.